AMENDMENT TO THE CLAIMS

Claim 1 (currently amended): A semiconductor device, ~~in which~~ including a semiconductor element with an integrated circuit ~~is~~ secured to a board,

wherein the semiconductor element is secured in a level position and specified to operate normally only when the semiconductor element is maintained in this level position,

wherein at least part of a back of the semiconductor element is subjected to surface processing and a stress is applied to the semiconductor element because of the surface processing, wherein the stress causes at least part of the semiconductor element ~~is~~ to deform~~ed~~ when being detached ~~the semiconductor element is detached~~ from the board, ~~due to the stress~~ whereby any reliable analysis of the semiconductor element is prohibited once the semiconductor element is detached from the board.

Claim 2 (original): The semiconductor device as defined in claim 1, wherein the semiconductor element is of a flipped-chip mounting type.

Claim 3 (cancelled).

Claim 4 (currently amended): The semiconductor device as defined in claim 1,

wherein the semiconductor element has a thickness of 50 μm or less in the area where the semiconductor element is surface processed.

Claim 5 (previously amended): The semiconductor device as defined in claim 1,

wherein the semiconductor element is specified to include a transistor section wherein transistors are provided at high density, the transistor section at least partially deforming convexly or concavely due to the stress when detached from the board.

Claim 6 (previously amended): The semiconductor device as defined in claim 1,

wherein the semiconductor element includes detector means for detecting an electrical property developing only when the semiconductor element is level, so as to control operation of the integrated circuit.

Claim 7 (currently amended): A method of manufacturing a semiconductor device, comprising the steps of:

(i) securing a semiconductor element having an integrated circuit to a board so that the semiconductor element is maintained in a level position;

(ii) subjecting at least a part of a back of the semiconductor element to surface processing, wherein the surface processing applies a stress to the semiconductor element, the stress causing at least a part of the semiconductor element to deform when being removed from the board,

wherein the semiconductor element only operates normally ~~only~~ when the semiconductor device is maintained in the board in ~~a~~ the level non-deforming position.

Claim 8 (previously amended): The method of manufacturing a semiconductor device as defined in claim 7,

wherein the step (ii) is specified to be carried out by at least one technique selected from a group consisting of scraping by means of dicing, sand blast, and sandpaper and treatment by means of laser beam projection.

Claim 9 (currently amended): The method of manufacturing a semiconductor device as defined in claim 7, wherein the step (ii) results in the semiconductor element having a thickness of 50 μm or less where the semiconductor element is surface processed.

Claim 10 (currently amended): A semiconductor device including a semiconductor element secured to a board, comprising:

a detector circuit section for detecting detachment of the semiconductor element from the board; and

an operation prohibition circuit section for prohibiting operation of the semiconductor element when the detector circuit section has detected the detachment of the semiconductor element from the board.

Claim 11 (currently amended): The semiconductor device as defined in claim 10, wherein:

the semiconductor element is specified to deform when being detached from the board; and

the detector circuit section is specified to detect the detachment of the semiconductor element from the board through detection of the deformation of the semiconductor element.

Claim 12 (currently amended): The semiconductor device as defined in claim 11, wherein:

the semiconductor element includes a transistor having an electrical property that ~~changing~~ changes according to the deformation of the semiconductor element; and

the detector circuit section is specified to detect the deformation of the semiconductor element through detection of the change in the electrical property of the transistor.

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Claim 13 (currently amended): The semiconductor device as defined in claim 12, wherein:

the detector circuit section is specified to output an operation signal to the operation prohibition circuit section when the electrical property of the transistor ~~does not~~ is unchanged from its normal operating status and ~~to stop~~ ceases the output of the operation signal when the electrical property of the transistor changes; and

the operation prohibition circuit section ~~is specified~~ does not ~~to~~ prohibit the operation of the semiconductor element ~~only~~ while receiving the operation signal.

Claim 14 (original): The semiconductor device as defined in claim 12, wherein the transistor is of either an NMOS or PMOS type.

Claim 15 (currently amended): The semiconductor device as defined in claim 10, wherein the operation prohibition circuit section is specified to prohibit operation of an integrated circuit provided in the semiconductor element.

Claim 16 (currently amended): The semiconductor device as defined in claim 10, wherein the detector circuit section and the operation prohibition circuit section are formed on the semiconductor element.

Claim 17 (currently amended): The semiconductor device as defined in claim 11, wherein the semiconductor element, when secured to the board, receives ~~such~~ a stress that could ~~otherwise~~ deform the semiconductor element when it is being detached from the board.

Claim 18 (original): The semiconductor device as defined in claim 17, wherein the semiconductor element is at least partially subjected to rough surface processing when the semiconductor element is secured to the board.

Claim 19 (original): The semiconductor device as defined in claim 18, wherein the semiconductor element has a thickness of 50 μm or less where the semiconductor element is subjected to the rough surface processing.

Claim 20 (original): The semiconductor device as defined in claim 18, wherein the semiconductor element has a thickness of 30 μm to 50 μm where the semiconductor element is subjected to the rough surface processing.

21. (currently amended): A semiconductor device, in which a semiconductor element with an integrated circuit is secured to a board,

wherein the semiconductor element is secured in a level non-deforming position and specified to operate normally only when the semiconductor element is maintained in this level position,

wherein the semiconductor element includes detector means for detecting an electrical property ~~developing~~ within the semiconductor element only when the semiconductor element is maintained in the level non-deforming position, so as to control operation of the integrated circuit.

Claim 22 (currently amended): A method of manufacturing a semiconductor device, comprising the steps of:

(a) securing a semiconductor element having an integrated circuit to a board so that the semiconductor element is maintained in a level non-deforming position;

(b) subjecting at least a part of a back of the semiconductor element to surface processing, wherein the surface processing applies a stress to the semiconductor element, the stress causing at least a part of the semiconductor element to deform when being removed from the board,

wherein the step (b) is specified to be carried out by at least one technique selected from a group consisting of scraping by means of dicing, sand blast, and sandpaper and treatment by means of laser beam projection.